REMARKS

This communication is a full and timely response to the aforementioned non-final Office Action dated July 10, 2007. By this communication, claims 1, 3 and 7 are amended. Claims 4, 6, 8 and 9 are not amended and remain in the application. Thus, claims 1, 3, 4 and 6-9 are pending in the application. Claim 3 is independent.

Reexamination of the application and withdrawal of the rejections of the claims are respectfully requested in view of the foregoing amendments and the following remarks.

I. Interview Request

Applicants' undersigned representative left several voicemails for the Examiner to request an interview prior to the filing of this response. The Examiner is respectfully requested to contact the undersigned upon consideration of this response to arrange for an interview.

II. Rejections under 35 U.S.C. § 112

Claims 1, 3, 4 and 6-9 were rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite. In particular, the Office asserted that the limitation "a module that does not have a maximum number of word lines" in claim 3 could be interpreted as reciting that the number of word lines in a module reaches toward infinity.

In response to this rejection, claim 3 has been amended to recite that "said plurality of modules have a different number of word lines from each other such that one of said plurality of modules has a finite maximum number of word lines." In addition, claim 3 has been amended to recite "said control circuit included in one of said modules that does not have the maximum number of word lines among said plurality of modules...."

Accordingly, Applicants respectfully submit that the indefiniteness rejection of claim 3 has been overcome by reciting that one of the plurality of modules has a finite maximum number of word lines, which precludes the above indefinite interpretation.

Therefore, Applicants respectfully request that the indefiniteness rejection of claims 1, 3, 4 and 6-9 be withdrawn.

III. Rejections under 35 U.S.C. § 103(a)

A. Claims 1, 3, 4 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamata (U.S. Patent Application Publication No. 2001/0042231) in view of Woods et al. (U.S. Patent No. 4,245,299, hereinafter "Woods"). This rejection is respectfully traversed for the following reasons.

Claim 3 recites a semiconductor integrated circuit comprising a plurality of modules having their operations controlled by respective chip select signals, and that each of the plurality of modules has a control circuit controlling an operation of reading or writing data from or into the memory cell, respectively. In addition, claim 3 recites that the plurality of modules have a different number of word lines from each other such that one of the plurality of modules has a finite maximum number of word lines.

Furthermore, claim 3 recites that the control circuit included in one of the modules that does not have the maximum number of word lines among the plurality of modules controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values.

Kawamata discloses a plurality of fail information memories 110-113 for a main memory array and one fail information memory 20 for redundant cells, where each memory 110-113 and 20 has addresses A0-A21 (see Figure 5). With reference to claim 3 of Kawamata, the Office asserted that Kawamata the memories 110-113 and 20 each have their own control circuit. This assertion is not supportable for the following reasons.

First, claim 3 of Kawamata merely recites "control means for writing fail information into said redundant cell fail information memory at said redundant cell fail information memory address." Claim 3 of Kawamata depends from claim 2, which expressly limits the memory testing apparatus to "one redundant cell fail information memory." Accordingly, at best, claim 3 of Kawamata merely discloses that the fail information memory 20 has a control means. Contrary to the Office's assertion,

Kawamata does not disclose or suggest that each of the fail information memories 110-113 and 20 has a control circuit.

Instead, Kawamata merely discloses that both channel data bits D0-D3 and a redundant signal are input to the main memories 110-113 and the memory 20. Accordingly, Applicants respectfully submit that Kawamata does not disclose or suggest a plurality of modules each having a control circuit, as recited in claim 3.

Kawamata merely discloses that a fail signal of the channel data bit D0 is supplied to a chip select terminal (CSB) in order to indicate whether information should be written into the module (see paragraph [0057]). This disclosure, however, has no relation to any address signal. Accordingly, Kawamata does not disclose or suggest a control circuit included in one of the modules that does not have the maximum number of word lines among the plurality of modules controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, as recited in claim 3.

In particular, Kawamata does not disclose or suggest that each of the memories 110-113 and 20 has a control circuit. Therefore, Kawamata does not disclose or suggest the above-described features of the control circuit that does not have the maximum number of word lines. Furthermore, as described above, each of the memories has the same number of address A0-A21. Therefore, as acknowledged by the Office, Kawamata does not disclose or suggest that the plurality of modules have a different number of word lines.

In an attempt to arrive at the subject matter of claim 1, the Office referred to paragraph [0061] of Kawamata, which discloses that a redundancy signal is supplied to an inverter 50, which outputs an inverted redundancy signal to a write enable (WEB) terminal of the fail information memory 20 (see paragraph [0061]). However, similar to paragraph [0057], the disclosure of paragraph [0061] does not disclose or suggest that a control circuit included in one of the modules that does not have the maximum number of word lines among the plurality of modules controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, as recited in claim 3.

As acknowledged by the Office, Kawamata does not disclose or suggest a plurality of modules that have a different number of word lines. In an attempt to cure the deficiencies of Kawamata, the Office applied Woods.

However, similar to Kawamata, Woods does not disclose or suggest that each of a plurality of modules has a control circuit, as recited in claim 3. In addition, similar to Kawamata, Woods does not disclose or suggest that a control circuit included in one of the modules that does not have the maximum number of word lines among the plurality of modules controls an operation of reading or writing data from or to said memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, as recited in claim 3.

Therefore, Woods cannot cure the deficiencies of Kawamata for failing to disclose or suggest each and every recited feature of claim 3.

Consequently, no obvious combination of Kawamata and Woods would result in the subject matter of claim 3, since Kawamata and Woods, either individually or in combination, do not disclose or suggest each and every recited feature of claim 3.

Furthermore, in view of the clear distinctions discussed above, one skilled in the art would not have reason or been motivated to modify Kawamata and Woods in such a manner as to result in, or otherwise render obvious, the subject matter of claim 3.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that claim 3 is patentable over Kawamata and Woods.

B. Claims 7-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawamata and Woods and further in view of Urakawa (U.S. Patent No. 6,324,106).

As demonstrated above, Kawamata and Woods fail to disclose or suggest all the recited features of independent claim 3. Applicants respectfully submit that Urakwa does not cure the deficiencies of Kawamata and Woods for failing to disclose or suggest that each of the plurality of modules has a control circuit, and that a control circuit included in one of the modules that does not have the maximum number of word lines among the plurality of modules controls an operation of reading

or writing data from or to said memory cell in a test mode, irrespective of a value of the chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values, as recited in claim 3.

Consequently, no obvious combination of Kawamata, Woods and Urakawa would result in the subject matter of claim 3, since these references, either individually or in combination, fail to disclose or suggest all the recited features of at least claim 3.

Therefore, for at least the foregoing reasons, Applicants respectfully submit that claim 3, as well as claims 1, 4 and 6-9 which depend therefrom, are allowable over the applied references.

IV. Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that the present application is clearly in condition for allowance. Accordingly, Applicants request a favorable examination and consideration of the instant application.

If, after reviewing this Amendment, the Examiner feels there are any issues remaining which must be resolved before the application can be passed to issue, the Examiner is respectfully requested to contact the undersigned by telephone in order to resolve such issues.

Respectfully submitted,

BUCHANAN INGERSOLL & ROONEY PC

Date: January 9, 2008

By: 
Jonathan R. Bowser
Registration No. 54574

P.O. Box 1404
Alexandria, VA 22313-1404
703 836 6620